CLAIMS

What is claimed is:

1. A method for writing a data bit to a memory array, said method comprising:

receiving a first input causing an application of high power, via a sense line, to an addressed bit in said memory array and causing a write operation on said addressed bit, and

receiving a second input causing an application of low power, via said sense line, to said addressed bit and causing a read operation on said addressed bit, such that said sense line is used to read and write said addressed bit.

2. The method as recited in Claim 1 further comprising addressing said addressed bit, via a plurality of address lines comprising a plurality of column address lines and a plurality of row address lines, provided said plurality of column address lines are high and said plurality of row address lines are low.

3. The method as recited in Claim 1 further comprising isolating a second plurality of switches, subsequent to the receiving of said first input, wherein said second plurality of switches are in a non-conductive state.

4. The method as recited in Claim 1 further comprising isolating a first plurality of switches, subsequent to the receiving of said second input, wherein said first plurality of switches are in a non-conductive state.

5. The method as recited in Claim 1 further comprising holding a voltage, determined at a plurality of nodes coupled to a first plurality of switches and a second plurality of switches, at a mid-voltage level, such that a zero state of said addressed bit is unchanged, said mid-voltage level provided by a plurality of sense amplifiers, coupled to said sense line.

6. The method as recited in Claim 1 further comprising changing a state of said addressed bit from a high resistance state to a low resistance state when said addressed bit is an anti-fuse.

7. The method as recited in Claim 1 further comprises changing a state of said addressed bit from a low resistance state to a high resistance state when said addressed bit is a fuse.

8. The method as recited in Claim 2 further comprising utilizing power-striping as part of said addressing of said addressed bit.

9. A circuit for writing a data bit to a memory array comprising:

a power source for providing voltage potential and current to said circuit and coupled thereto;

a input line for receiving inputted data bit values and coupled to a logic inverter;

a plurality of first transistors having first leads coupled to said input line;

a plurality of second transistors having first leads coupled to an output of said logic inverter;

a plurality of sense lines coupled to other leads of said first and said second plurality of transistors and coupled to said memory array;

a plurality of sense amplifiers coupled to other leads of said first and said second plurality of transistors; and

a plurality of address lines coupled to said memory array and coupled to said sense lines, enabling writing of said data bit to an addressed bit of said memory array.

10. The circuit of Claim 9 wherein said first plurality of transistors comprise a first transistor and a fourth transistor, and wherein a third lead of said first transistor is coupled to a higher potential voltage coupled to said circuit, and wherein a second lead of said first transistor is coupled to one of said plurality of sense lines.

11. The circuit of Claim 10 wherein a second lead of said fourth transistor is coupled to a lower potential voltage coupled to said circuit, and

wherein a third lead of said fourth transistor is coupled to one of said sense lines.

12. The circuit of Claim 9 wherein said plurality of second transistors comprise a second transistor and a third transistor, and wherein a third lead of said second transistor is coupled to one of said plurality of sense lines, and wherein a second lead of said second transistor is coupled to a input of one of said plurality sense amplifiers.

13. The circuit of Claim 12 wherein a third lead of said third transistor is coupled to an input of one of said sense amplifiers and wherein a second lead of said third transistor is coupled to one of said sense lines.

14. The circuit of Claim 9 wherein said plurality of sense lines comprise a row sense line and a column sense line and wherein said row sense line is coupled to a second lead of a third transistor of said second plurality of transistors and wherein said row sense line is coupled to a third lead of a fourth transistor of said first plurality of transistors.

15. The circuit of Claim 14 wherein said column sense line is coupled to a second lead of a first transistor of said first plurality of transistors and wherein said column sense line is coupled to a third lead of a second transistor of said second plurality of transistors.

16. The circuit of Claim 9 wherein said plurality of sense amplifiers comprise an column sense amplifier and a row sense amplifier and wherein an input of said column sense amplifier is coupled to a second lead of a second transistor of said second plurality of transistors.

17. The circuit of Claim 16 wherein an input of said row sense amplifier is coupled to a third lead of a third transistor of said second plurality of transistors.

18. The circuit of Claim 9 wherein said plurality of address lines comprise a plurality of row address lines and a plurality of column address

lines, and when said plurality of row address lines are of a low voltage and when said plurality of column address lines are of a high voltage, addressing of said addressed bit of said memory array is enabled.

19. The circuit of Claim 9 wherein said writing of said data bit to said addressed bit of said memory array changes the state of said addressed bit from a high resistance state to a low resistance state when said addressed bit is an anti-fuse, and wherein writing of said data bit to said addressed bit of said memory array changes the state of said addressed bit from a low resistance state to a high resistance state when said addressed bit is a fuse.

20. The circuit of Claim 18 wherein power striping is used as part of said addressing of said addressed bit.

21. A circuit for writing a data bit to an addressed bit in a memory array comprising:

a power source for providing voltage potential and current to said circuit and coupled thereto;

a data bit input line for receiving inputted data bit values and coupled to a logic inverter;

a first transistor having a first lead coupled to said data input line and a second lead coupled to a column sense line and a third lead coupled to a positive voltage, said positive voltage coupled to said circuit;

a second transistor having a first lead coupled to an output of said logic inverter and a second lead coupled to an input of a column sense amplifier and a third lead coupled to said column sense line;

a third transistor having a first lead coupled to said output of said logic inverter and a second lead coupled to a row sense line and a third lead coupled to an input of a row sense amplifier; and

a fourth transistor having a first lead coupled to said input line and a second lead coupled to a negative voltage and a third lead coupled to said row address line, enabling writing of said data bit to said addressed bit.

22. The circuit of Claim 21 further comprising a plurality of column address lines coupled to said memory array and coupled to said column sense

line and a plurality of row address lines coupled to said row sense line, and wherein addressing said addressed bit of said memory is enabled when said plurality of column address are of a positive voltage and when said plurality of said row address lines are of a negative voltage.

23. The circuit of Claim 21 wherein said addressed bit is written to a one state when said state of said addressed bit is changed from a high resistance state to a low resistance state when said addressed bit is an anti-fuse and when said state of said addressed bit is changed from a low resistance state to a high resistance state when said addressed bit is a fuse.

24. The circuit of Claim 21 wherein said addressed bit is written to a zero when said row sense amplifier, coupled in feedback, and said column sense amplifier, coupled in feedback, disable writing of one bit by holding said voltage potential at a mid-voltage, such that said addressed bit remains a zero by not writing a one bit.

25. The circuit of Claim 22 wherein power striping is utilized in part of said addressing said addressed bit.

26. A circuit for writing a data bit to a memory array comprising:

a power source for providing voltage potential and current to said circuit and coupled thereto;

a input line for receiving inputted data bit values and coupled to said memory array;

a plurality of first transistors having first leads coupled to said input line;

a plurality of second transistors having first leads coupled to said input line, and wherein said plurality of second transistors are complimentary to the polarity of said plurality of first transistors;

a plurality of sense lines coupled to other leads of said first and said second plurality of transistors and coupled to said memory array;

a plurality of sense amplifiers coupled to other leads of said first and said second plurality of transistors; and

a plurality of address lines coupled to said memory array and coupled to said sense lines, enabling writing of said data bit to an addressed bit of said memory array.

27. The circuit of Claim 26 wherein said first plurality of transistors comprise a first transistor and a fourth transistor, and wherein a third lead of said first transistor is coupled to a higher potential voltage coupled to said circuit, and wherein a second lead of said first transistor is coupled to one of said plurality of sense lines.

28. The circuit of Claim 27 wherein a second lead of said fourth transistor is coupled to a lower potential voltage coupled to said circuit, and wherein a third lead of said fourth transistor is coupled to one of said sense lines.

29. The circuit of Claim 26 wherein said plurality of second transistors comprise a second transistor and a third transistor, and wherein a third lead of said second transistor is coupled to one of said plurality of sense lines, and wherein a second lead of said second transistor is coupled to a input of one of said plurality sense amplifiers.

30. The circuit of Claim 29 wherein a third lead of said third transistor is coupled to an input of one of said sense amplifiers and wherein a second lead of said third transistor is coupled to one of said sense lines.

31. The circuit of Claim 26 wherein said plurality of sense lines comprise a row sense line and a column sense line and wherein said row sense line is coupled to a second lead of a third transistor of said second plurality of transistors and wherein said row sense line is coupled to a third lead of a fourth transistor of said first plurality of transistors.

32. The circuit of Claim 31 wherein said column sense line is coupled to a second lead of a first transistor of said first plurality of transistors and wherein said column sense line is coupled to a third lead of a second transistor of said second plurality of transistors.

33. The circuit of Claim 26 wherein said plurality of sense amplifiers comprise an column sense amplifier and a row sense amplifier and wherein an input of said column sense amplifier is coupled to a second lead of a second transistor of said second plurality of transistors.

34. The circuit of Claim 33 wherein an input of said row sense amplifier is coupled to a third lead of a third transistor of said second plurality of transistors.

35. The circuit of Claim 26 wherein said plurality of address lines comprise a plurality of row address lines and a plurality of column address lines, and when said plurality of row address lines are of a low voltage and when said plurality of column address lines are of a high voltage, addressing of said addressed bit of said memory array is enabled.

36. The circuit of Claim 26 wherein said writing of said data bit to said addressed bit of said memory array changes the state of said addressed bit from a high resistance state to a low resistance state when said addressed bit is an anti-fuse, and wherein writing of said data bit to said addressed bit of said memory array changes the state of said addressed bit from a low resistance state to a high resistance state when said addressed bit is a fuse.

37. The circuit of Claim 35 wherein power striping is used as part of said addressing of said addressed bit.

38. A system for writing a data bit to a memory array, said method comprising:

means for receiving a first input causing an application of high power to an addressed bit in said memory array, via a sense line, and causing a write operation on said addressed bit, and

means for receiving a second input causing an application of low power to said addressed bit, via said sense line, and causing a read operation on said addressed bit, such that said sense line is used to read and write said addressed bit.

39. The system as recited in Claim 38 further comprising a means for addressing said addressed bit, via a plurality of address lines comprising a plurality of column address lines and a plurality of row address lines, provided said plurality of said column address lines are high and said plurality of said row address lines are low.

40. The system as recited in Claim 38 further comprising means for isolating a second plurality of switches, subsequent to the receiving of said first input, wherein said second plurality of switches are in a non-conductive state.

41. The system as recited in Claim 38 further comprising means for isolating a first plurality of switches, subsequent to the receiving of said second input, wherein said first plurality of switches are in a non-conductive state.

42. The system as recited in Claim 38 further comprising means for holding a voltage, determined at a plurality of nodes coupled to a first and a second plurality of switches, at a mid-voltage level, such that a zero state of said addressed bit is unchanged.

43. The system as recited in Claim 38 further comprising means for changing a state of said addressed bit from a high resistance state to a low resistance state when said addressed bit is an anti-fuse.

44. The system as recited in Claim 38 further comprises means for changing a state of said addressed bit from a low resistance state to a high resistance state when said addressed bit is a fuse.

45. The system as recited in Claim 39 further comprising means for utilizing power-striping as part of said addressing of said addressed bit.